**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of the claims in the application:

**Listing of Claims:**

1. (Currently Amended) A photodetecting array comprising:

a plurality of detecting cells laid out in an array on a substrate, comprising rows and columns of detecting cells;

a plurality of gate lines, wherein each of the gate lines are coupled to a different row of more than two detecting cells;

a plurality of data lines, wherein each of the data lines are coupled to a different column of more than two detecting cells;

a mesh of bias voltage lines, comprising a plurality of additional bias voltage lines and a plurality of main bias voltage lines, wherein each of the additional bias voltage lines are coupled between at least a pair of main bias voltage lines;

~~a plurality of main bias voltage lines,~~ wherein each of the main bias voltage lines are coupled to a different row of more than two detecting cells; and

~~a plurality of additional bias voltage lines, wherein each of the additional bias voltage lines are coupled to two main bias voltage lines in different rows,~~ wherein the gate lines and main bias voltage lines are laid out in a plurality of rows and the data lines and additional bias voltage lines are laid out in a plurality of columns.

2. (Original) A photodctecting array as in claim 1 wherein each of said plurality of detecting cells comprises a transistor and a photodiode, and wherein one of said plurality of gate lines is coupled to said transistor and one of said plurality of data lines is coupled to said transistor.

3. (Original) A photodetecting array as in claim 2 wherein said photodiode comprises:

an n+ layer formed over a first passivation layer;

an amorphous silicon layer formed over said n+layer;

a p+layer formed over said amorphous silicon layer; and

a conductive layer formed over said p+layer.

4. (Original) A photodetecting array as in claim 2 wherein each photodiode in said array is segmented from other photo diodes in said array.

5. (Original) A photodetecting array as in claim 4 wherein said photodiode in a cell is disposed above said transistor in said cell.

6. (Cancelled)

7. (Cancelled)

8. (Previously Presented) A photodetecting array as in claim 5 wherein each said photodiode comprises:

a n+layer formed over a first passivation layer;
an amorphous silicon layer formed over said n+layer;
a p+layer formed over said amorphous silicon layer; and
a conductive layer formed over said p+layer.

9. (Currently Amended) A photodetecting array as in claim 1 wherein said plurality of main bias voltage lines and plurality of additional bias voltage lines, together, form a staircase grid of bias voltage lines comprises a first plurality of main bias voltage lines which are laid out parallel to and proximate to corresponding gate lines and a second plurality of additional bias voltage lines which are laid out parallel to and proximate to only a portion of said plurality of data lines, said second plurality of additional bias voltage lines being coupled electrically between said first plurality of main bias voltage lines.

10. (Currently Amended) A photodetecting array as in claim 9 wherein a capacitive coupling between said second plurality of additional bias voltage lines and said plurality of data lines is limited substantially to said portion.

11. (Currently Amended) A photodetecting device comprising:

a first row of more than two detecting cells, each having a transistor and a photodiode;

a second row of more than two detecting cells, each having a transistor and a photodiode, said second row being adjacent to and parallel with said first row;

a first gate line coupled to said first row;

a second gate line coupled to said second row;

a mesh of bias voltage lines, comprising additional bias voltage lines and main bias voltage lines, wherein each of the additional bias voltage lines are coupled between at least a pair of main bias voltage lines; wherein the main bias voltage lines comprises:

a first main bias voltage line laid out parallel with and proximate to said first gate line and coupled to more than two detecting cells in said first row; and

a second main bias voltage line laid out parallel with and proximate to said second gate line and coupled to more than two detecting cells in said second row; and

wherein the additional bias voltage lines comprises:

a third additional bias voltage line laid out parallel with and proximate to a first data line, said third additional bias voltage line being electrically coupled between said first main bias voltage line and said second main bias voltage line;

wherein the capacitive coupling between the mesh of bias voltage lines and the data lines is substantially limited to the capacitive coupling between the third additional bias voltage line and the first data line.

12. (Previously Presented) A photodetecting device as in claim 11 wherein said first and said second main bias voltage lines provide a reverse bias voltage to photodiodes in said first row of detecting cells and in said second row of detecting cells.

13. (Cancelled).

14. (Currently Amended) A photodetecting device as in claim 11, ~~13~~ further comprising:

a second data line; and

a fourth additional bias voltage line laid out parallel with and proximate to said second data line, said fourth additional bias voltage line being electrically coupled to said second main bias voltage line and to a fifth main bias voltage line.

15. (Previously Presented) A photodetecting device as in claim 14 wherein said first data line and said second data line are laid out substantially perpendicular to said first gate line and to said second gate line and wherein said third additional bias voltage line is not coupled to said fifth main bias voltage line and wherein said fourth additional bias voltage line is not coupled to said first main bias voltage line.

16. (Original) A photodetecting device as in claim 15 wherein said first gate line is coupled to transistors in said first row of detecting cells and said second gate line is coupled to transistors in said second row of detecting cells.

17. (Original) A photodetecting device as in claim 11 wherein each photodiode in said first row and in said second row of detecting cells is segmented from other photodiodes.

18. (Original) A photodetecting device as in claim 17 wherein said photodiode in a cell is disposed above said transistor in said cell.

19. (Original) A photodetecting device as in claim 18 wherein each said photodiode comprises:

an n+layer formed over a first passivation layer;

an amorphous silicon layer formed over said n+layer;

a p+layer formed over said amorphous silicon layer; and

a conductive layer formed over said p+layer.

20. (Currently Amended) A photodetecting array comprising:

a plurality of detecting cells laid out in an array on a substrate, wherein said array comprises rows and columns of detecting cells, wherein each of the said detecting cells comprising a photodiode and a transistor;

a plurality of gate lines laid out parallel to the rows of the array, wherein each of the gate lines are coupled to one of said rows of more than two detecting cells;

a plurality of data lines laid out parallel to the columns of the array, wherein each of the data lines are coupled to one of said columns of detecting cells;

a mesh of bias voltage lines, said mesh comprising first main bias voltage lines disposed in a first direction which is laid out substantially parallel to said gate lines and second additional bias voltage lines disposed in a second direction which is laid out substantially perpendicular to said gate lines,

wherein each of the additional bias voltage lines are coupled between at least a pair of main bias voltage lines, ~~and~~

wherein a total length of said first main bias voltage lines exceeds a total length of said second additional bias voltage lines, and

wherein the capacitive coupling between the bias voltage lines and the data lines is proportional to the total length of the second additional bias voltage lines.

21. (Currently Amended) A photodetecting array as in claim 20 wherein said total length of said first main bias voltage lines greatly exceeds said total length of said second additional bias voltage lines by a factor of at least 10 times, and wherein said first main bias voltage lines are proximate to corresponding said gate lines.

22. (Currently Amended) A method for manufacturing a photodetecting array, said method comprising:

forming a plurality of gate lines;

forming a plurality of transistor structures laid out in an array, the array comprising rows and columns;

forming a plurality of data lines laid out in columns, wherein the data lines are coupled to said transistor structures laid out in columns of the array;

forming a plurality of photodiode structures over the transistors;

forming a mesh of bias voltage lines, said mesh comprising first main bias voltage lines disposed in a first direction which is laid out substantially parallel to and proximate to said gate lines and second additional bias voltage lines disposed in a second direction which is laid out substantially perpendicular to said gate lines,

wherein each of the additional bias voltage lines are coupled between at least a pair of main bias voltage lines, ~~and~~

wherein a total length of said first main bias voltage lines exceeds a total length of said second additional bias voltage lines, and

wherein the capacitive coupling between the bias voltage lines and the data lines is proportional to the total length of the second additional bias voltage lines.

23-29. (Cancelled)

30. (Previously Presented) The photodetecting array of claim 1, wherein the total length of the additional bias voltage lines are substantially less than the total length of the main bias voltage lines.

31. (Previously Presented) The photodetecting array of claim 2, wherein the transistor is coupled to the gate line by a first pathway and to the data line by a second pathway, and wherein the photodiode is coupled to the transistor by a third pathway and to the main bias voltage line by a fourth pathway, wherein the first, second, third, and fourth pathways are all distinct and separate from each other.

32. (Previously Presented) The photodetecting array of claim 31, wherein the main bias voltage lines are laid out parallel to the gate lines and perpendicular to the data lines.

33. (Previously Presented) The photodetecting array of claim 1,

wherein the capacitive coupling between the plurality of bias voltage lines and the data lines are limited substantially to the proportional length of the additional bias voltage lines to the total length of the plurality of bias voltage lines; and

wherein the additional bias voltage lines substantially reduces the resistance of the main bias voltage lines.

34. (Previously Presented) The photodetecting array of claim 20,

wherein the capacitive coupling between the plurality of bias voltage lines and the data lines are limited substantially to the proportional length of the additional bias voltage lines to the total length of the plurality of bias voltage lines.

35. (Previously Presented) The photodetecting array of claim 21,

wherein the capacitive coupling between the plurality of bias voltage lines and the data lines are limited substantially to the proportional length of the additional bias voltage lines to the total length of the plurality of bias voltage lines; and

wherein the additional bias voltage lines substantially reduces the resistance of the main bias voltage lines.

36. (Previously Presented) The photodetecting array of claim 11, wherein the transistor is coupled to the gate line and the data line, and wherein the photodiode is coupled to the transistor and the main bias voltage line.

37. (Previously Presented) The photodetecting array of claim 20, wherein the transistor is coupled to the gate line and the data line, and wherein the photodiode is coupled to the transistor and the main bias voltage line.

38. (Previously Presented) A photodetecting array comprising:

a plurality of detecting cells laid out in an array on a substrate, wherein said array comprises rows and columns of detecting cells, wherein each of the said detecting cells comprising a photodiode and a transistor;

a plurality of gate lines laid out parallel to the rows of the array, wherein each of the gate lines are coupled to one of said rows of more than two detecting cells;

a plurality of data lines laid out parallel to the columns of the array, wherein each of the data lines are coupled to one of said columns of detecting cells;

a mesh of bias voltage lines, comprising additional bias lines and main bias lines, wherein each of the additional bias lines are coupled between at least a pair of main bias lines;

the mesh having a means for limiting the capacitive coupling between the bias voltage lines and the data lines.